REMARKS

Claims 63-73 are pending in the present application. Claims 63-68 were rejected and claims 69-73 were allowed in the Office Action dated November 2, 2004. Reconsideration of claims 63-68 is respectfully requested in light of the arguments presented below.

Claim 63 was rejected under 35 USC 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Office Action indicated that the preamble, "A semiconductor disk device, comprising," limited subsequent claim elements to being part of EEPROM array 33, and that this configuration was not enabled. It is not clear why the preamble is given such weight and it is submitted that the particular meaning attributed to the preamble is contrary to its ordinary meaning. It is submitted that the claimed configuration is not limited as indicated by the Office Action and that the configurations of the specification fully support the claims.

"[A] claim preamble has the import that the claim as a whole suggests for it." MPEP 2111.02 citing *Bell Communications*. Here, the Office Action does not indicate what claim features suggest treating the preamble as an actual claim limitation. Furthermore, MPEP 2111.02 states, "The claim preamble must be read in the context of the entire claim. The determination of whether preamble recitations are structural limitations or mere statements of purpose or use 'can be resolved only on review of the entirety of the [record] to gain an understanding of what the inventors actually invented and intended to encompass by the claim." Here, the Office Action appears to construe the preamble in a way that is contrary to that indicated by the body of the claim. In particular, the claim recites, "a non-volatile, electronically programmable and erasable flash memory." Additional components are then recited, including, "interface means", "flash control buffer" and "access means." However, there appears to be no indication in the body of the claim that the additional components are within an EEPROM. Thus, it is not clear how such a meaning was suggested. Thus, no basis has been provided for treating the preamble as an actual claim limitation and the interpretation indicated in the Office Action does not appear to be suggested by the body of the claim.

Even if the preamble is given the weight of a claim limitation, it is submitted that a reasonable interpretation of the claim with this limitation is fully supported by the specification. In particular, "A semiconductor disk device" is submitted to have an ordinary meaning that is not limited to an EEPROM memory array such as EEPROM array 33. Such an interpretation is supported throughout the specification. The specification describes, "substitution of a specific type of semiconductor memory system for the disk drive," page 6, lines 19-20. "The bulk storage memory 29 is constructed of a memory controller 31, connected to the computer system bus 23, and an array 33 of EEprom integrated circuit chips," page 6, lines 31-34. Thus, bulk storage memory 29 includes Eeprom chips and additional components. The Office Action appeared to concede that the individual limitations of the body of claim 63 were supported because the rejection was not based on the absence of the components of these limitations, but on the location of the components. Because the preamble is submitted not to be an actual claim limitation, or to be a limitation that does not limit the location of subsequent claim elements to being within an Eeprom memory array, it is submitted that all actual claim limitations are supported.

In particular, "flash control buffer means for performing data exchange between the flash memory and the interface means" is supported for example in Fig. 1B, interface 40; Fig 3A, interface 227; Figs 6 and 7, receiver 313, FIFO 519 and FIFO 601; Fig. 8, cache 705. While these examples show some locations for a flash control buffer that are outside an EEPROM array (as noted in the Office Action), claim 63 is not believed to be limited to a location within an EEPROM array and therefore this limitation is submitted to be supported.

"Access means for converting a sector address received from the external system into a substitute address and for accessing the flash memory according to the substitute address" is supported in Fig 1B, controller 31 and interface 40; Figs. 2 and 3A, p.9, line 10 through p.11, line 6; Figs 6 and 7, p.17, line 25 through p.24, line 30. While these examples show some locations for access means that are outside an EEPROM array (as noted in the Office Action), claim 63 is not believed to be limited to a location within an EEPROM array and therefore this limitation is submitted to be fully supported.

The Office Action also stated that there was insufficient support for the "access means" limitation because, "Fig. 1B and Figs 6-8 do not show the access means for converting." The Office Action stated with respect to Figure 3A, "This block diagram circuit 220 has a decoder for decoding the address, not converting the address." However, the distinction between decoding and converting as explained in the Office Action is not understood. It appears that decoding is an example of converting an address from one form (encoded) to another form (unencoded). Thus, decoding provides support for the term "converting" used in claim 63.

Another example of address conversion in the present application is provided by address mapping to replace defective sectors with substitute sectors. "When the number in a sector exceeds a predetermined value, the controller marks that sector as defective and maps it to another sector," page 23, lines 17-19. The Office Action indicated that this was not an access means for converting because, "The access means for converting a sector address into a logical block address converts **all** the sector addresses into a logical block address," Office Action page 6, lines 9-11. However, no such limitation appears in claim 63. Claim 63 recites, "converting **a** sector address... into **a** substitute address." Claim 63 does not refer to "all the sector addresses." Therefore, it is submitted that an example of an access means for converting according to claim 63 is shown by this mapping and thus, the limitation is supported.

Claim 65 was rejected under 35 USC 112 as lacking support for the limitation, "the substitute address includes a logical block address." The Office Action stated that "the logical block address is the address for every block." However, no such limitation is recited in claim 65. Claim 65 simply recites "**the** substitute address includes **a** logical block address." There appears to be no limitation in this claim that would limit the logical block address to being the address for every block in the semiconductor disk device. Thus, claim 65 appears to be fully supported, for example at page 23, lines 17-19, as discussed above.

Claims 66-68 were rejected under 35 USC 112 as being indefinite because it was not clear what the data buffer is connected to. Claim 66 is amended to indicate that the data buffer is connected to the interface. Thus, claim 66 as amended is submitted to be definite.

Accordingly, it is submitted that all claims are fully supported and it is requested that the above rejections be withdrawn and an interference be declared as previously requested. However, if the Examiner is aware of any additional matters that should be discussed a phone call to the undersigned attorney at (415) 318-1160 would be appreciated.

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 2, 2005.

Franklin Dyer

Respectfully submitted,

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